UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,007	07/23/2003	Kyoung-woo Lee	SAM-0313CIP	8434

7590 05/24/2006

Steven M. Mills
MILLS & ONELLO LLP
Suite 605
Eleven Beacon Street
Boston, MA 02108

EXAMINER	
LEE, KYOUNG	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 05/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,007	LEE ET AL.	
	Examiner	Art Unit	
	Kyoung Lee	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3, 5-10, 13, 16, 18-28, 31, 34, 36-43, 45, 48, and 50-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsu et al. (U.S. Patent No. 6,461,955) in view of Jiang et al. (U.S. Patent Appl. No. 2002/0031906) and Aoi (U.S. Patent No. 6,387,824) and Lee et al. (U.S. Patent No. 6,171,951).

Referring to Figs. 2A-2G and related text, Tsu discloses [Re claim 1] a method of fabricating dual damascene interconnections, the method comprising: (a) forming on a substrate 100 a hybrid dielectric layer 106, 108; (b) forming a via 112 in the dielectric

layer; (c) filling the via with a carbon-free inorganic filler 114; (e) partially etching the inorganic filler filling the via and the dielectric layer to form a trench, which is connected to the via and in which interconnections will be formed (see Fig. 2E); (f) removing the inorganic filler remaining in the via; and (g) completing interconnections by filling the trench and the via with interconnection material (See Fee 2F-2G); [Re claims 2, 4-5, 10, 13, 21-23, and 31] a method of fabricating dual damascene interconnections, the method comprising: (a) forming a dielectric layer on a substrate; (b) forming a via in the dielectric layer; (c) filling the via with an HSQ-based filler (see col. 3, lines 29-39); (e) partially etching the HSQ -based filler filling the via and the dielectric layer to form a trench, which is connected to the via and in which interconnections will be formed; (f) removing the HSQ -based filler remaining in the via; and (g) completing interconnections by filling the trench and the via with an interconnection material, as shown above; [Re claims 3, 6-8, 24-27, and 40-43] the method wherein the etch stop layer is formed of at least one of SiC, SiN, and SiCN; before step (b), forming a capping layer on the dielectric layer having a dielectric constant of 3.3 or less; wherein in step (b), a via is formed in the capping layer and the dielectric layer; wherein the capping layer is formed of an anti-reflective material; wherein the capping layer is formed of at least one of SiO2, SiOF, SiON, SiC, SiN and SiCN (see Figs. 2A-2C and col. 2, line 45-co1. 3, line 14).

But Tsu et al. fails to disclose expressly the use of an organo silicate glass and the value of its dielectric constant, the etching of the filler using HF, the use of CVD to deposit an organo silicate glass, the processing the surface of the filler using plasma

and the details about the plasma. However, the missing limitations are well known in the art because Aoi discloses most of these features (See embodiment 3) and Lee discloses plasma treating a low k dielectric layer by plasma treatment, such as Ar, N_2, or N_2O to prevent dissolution of the carbon-free filler or HSQ-based filler and to densify the layer preventing damage caused by subsequent process (see col. 3, lines 24-37) and Jiang disclose the method of forming a dual damascene using organo silicate glass having a dielectric constant of 3.3 or less to minimized the power consumption (see paragraph [0008] and [0020]). Besides HF is well known to be used for etching silicon oxide based material. A person of ordinary skill is motivated to modify Tsu with Jiang, Aoi and Lee to obtain device of low capacitance made in a more reliable manner.

[Re claim 39] The combined teachings of Tsu, Jiang, Aoi, and Lee disclose the method as claimed and rejected in claims 21-23 also apply. Besides, Lee also discloses forming a hard mask 312 of silicon nitride or silicon oxynitride, which are also ARC material, on the plasma treated layer 310 (see Fig. 2B-2C).

[Re claims 16, 34, and 48] wherein step (d) includes: forming a photoresist pattern 120 on the inorganic filler to define the trench; forming the trench by dry etching using the photoresist pattern as an etch mask such that an etch ratio of the inorganic filler to the dielectric layer is 4:1 or lower; and removing the photoresist pattern (see column 3, lines 14-46).

[Re claims 18-19, 36-37, and 50-51] wherein step (f) comprises wet etching such that an etch ratio of the inorganic filler to the dielectric layer is 20:1 or higher (see Fig.

2D-2E and col. 3, lines 29-38); [Re claims 20, 38, and 52] wherein in step (g), the interconnection is a copper interconnection (see col. 4, lines 13-17).

[Re claims 9 and 28] Aoi also discloses forming a photoresist pattern on the dielectric layer to define the via; and forming the via exposing the etch stop layer by dry etching the dielectric layer using the photoresist pattern ms an etch mask (see Fig. 3(b)).

[Re claim 45] The combined teachings of Tsu, Jiang, Aoi, and Lee disclose the method as claimed and rejected in claims 13 and 31 also apply. Therefore, at the time of the invention, it would have been obvious to combine Tsu with Jiang, Aoi, and Lee to obtain the invention as specified in claims 1-10, 13, 16, 18-28, 31, 34, 36-43, 45, 48, and 50-52.

Claims 17, 35, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable Tsu in view of Jiang, Aoi, and Lee, as applied above, and further in view of Robinson et al. (U.S. Patent No. 4,201,579).

The combined teaching of Tsu, Jiang, Aoi and Lee discloses substantially the limitations of claims 17, 35, and 49, as shown above. Jiang also discloses the method wherein the dry etching uses CxFy or CxHyFz as a main etching gas (see paragraph [0027]), but Tsu, Jiang, Aoi and Lee fail to disclose expressly the method of removing the photoresist pattern using an H2-based plasma. However, the missing limitation is well known in the art because Robinson discloses the use of H2 plasma to remove photoresist (See col. 1, lines 52-65). A person of ordinary skill is motivated to modify Tsu, Aoi and Lee with Robinson to obtain clean device with no undesirable oxidation.

Therefore, at the time of the invention, it would have been obvious to combine Tsu, Jiang, Aoi, and Lee with Robinson to obtain the invention as specified in claims 17, 35, and 49.

Claims 11-12, 14-15, 29-30, 32-33, 44, and 46-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsu in view of Jiang, Aoi, Lee, and further in view of Lui (U.S. Patent No. 6,391,761).

The combined teaching of Tsu Jiang, Aoi, and Lee disclose substantially the limitations of claims 11-12, 14-15, 29-30, 32-33, 44, and 46-47, as shown above. But Tsu, Jiang, Aoi, and Lee, fail to disclose expressly the use of an organic antireflective layer under a photoresist layer. However, this feature is well known in the art because Lui discloses the use of an organic antireflective layer 85 (See par. bridging cols. 4-5). The combined teaching of Tsu, Jiang, Aoi, Lee and Lui does not disclose the thickness of the antireflective layer or the inclusion in the filler of a light absorption material and/or a dissolution inhibitor for a photoresist developing solution. However, it would have been obvious for an ordinary artisan to select an appropriate thickness to effectively achieve the desired objective and to include in the filler a dissolution inhibitor for a photoresist developing solution to prevent damage of the filler when the photoresist is developed. A person of ordinary skill is motivated to modify Tsu and the applied references with Lui to obtain better resolution. Therefore, at the time of the invention, it would have been obvious to combine Tsu and the applied references with Lui to obtain the invention as specified in claims 11-12, 14-15, 29-30, 32-33, 44, and 46-47.

Response to Arguments

In view of arguments and the amendment to the claims, the rejections of claims 1-52 under 35 U.S.C. 103, as stated in the immediately preceding Office Action, have been withdrawn.

Applicant' s arguments with regard to the rejections under 35 U.S.C. 103 has been fully considered, but they are not deemed to be persuasive for at least the following reasons.

Applicants argued that the combined teaching of Tsu with the applied references does not teach plasma treating the surface of the filler. The examiner disagreed, even though Lee does not expressly disclose plasma treating the surface of the low k filler however Lee discloses the benefits of plasma treating an exposed surface of a low k dielectric at least to prevent damage caused by subsequent processing, the examiner considers this benefit to be a teaching applicable to exposed surface of a low k dielectric susceptible to damage caused by a subsequent process; the damage would results in problem with accurate control of feature dimensions. An ordinary artisan would have been motivated to combine Lee with Tsu to have better control of feature dimensions. In the combined teaching of Tsu with the applied references the surface of the filler is treated with plasma then the etching of the plasma treated filler would give better control of thickness to be etched resulting in more accurate trench width and depth.

Applicants argued that Lee does not disclose the dissolution of the carbon-free filler or HSQ-based filler in processing. The examiner disagreed, even though Lee does

not expressly disclose plasma treating the surface of the low k filler in order to prevent dissolution of the carbon-free filler or HSQ-based filler, it would inherently prevent dissolution of the carbon-free filler or HSQ-based filler.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kyoung Lee whose telephone number is (571) 272-1982. The examiner can normally be reached on M-F 8:30AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KL 5/22/06

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER